

RESUME

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Education

- 1980-1983 University of Massachusetts, Amherst, U. S. A.
Ph.D. (Electrical and Computer Engineering)
Dissertation : "Monte Carlo simulation of MOSFET and Bipolar Transistors"
- 1975-1977 Seoul National University, Seoul, Korea
M.S. (Electrical Engineering)
Thesis : "MOS Capacitor Fabrication and Study on the Si-SiO₂ Interface"
- 1971-1975 Seoul National University, Seoul, Korea
B.S. (Electrical Engineering)

Experience

- 1997 - Professor, School of Electrical Engineering, Seoul National University,
Has advised 30 Ph.D. Students, 31 Master students.
- 2003 - Director of Nano Systems Institute_ National Core Research Center,
Seoul National University
- 2001-2002 Director, Hynix semiconductor, memory R&D
- 2000-2002 Director, Inter-university Semiconductor Research Center,

Seoul National University

- 1999-2001 Director of "A Collaborative Project for Excellence in Basic System ICTechnology"
- 1996-1998 Director of "National Project on Next Generation Semiconductor Technology"
- 1995-1997 Director, Inter-university Semiconductor Research Center, Seoul National University
- 1992-1997 Associate Professor, School of Electrical Engineering, Seoul National University
- 1988-1992 Assistant Professor, Dept. of Electronics Engineering, Seoul National University
- 1992-1993 Visiting Scholar, Integrated Circuit Laboratory, Stanford University
- 1985-1988 Principal Scientist, Gold Star Semiconductor R&D, Korea, developed high performance CMOS and BiCMOS technology
- 1983-1985 Researcher, IBM, East Fishkill, New York , developed advanced modeling for bipolar technology used for the next generation IBM main computer
- 1977-1980 Instructor, Korea Naval Academy, Jinhae, Korea, taught physical electronics, circuit theory and logic design; developed finite element analysis program for bipolar transistors

Awards/Honors

1. The award of republic of Korea naval academy (1979)
2. The award of the president of LG cooperation for developing 4MD DRAM(1986)
3. The best teacher award : Seoul National University (1999)
4. Tin Tower Order of Industrial Service Merit: President of Korea (2002)
5. Member of NAEK (National Academy of Engineers of Korea)(from 2004)
6. The award of Role Model Scientist (KOFAC 2008)

Contributions to Industry

Director of Memory R&D of Hynix Semiconductor, Inc.,(2000-2002) on leave of absence from Seoul National University.

As the Director of R&D with more than 2000 engineers under his supervision, he led the 'blue chip' project for 256MDRAM family to make the DRAM process most efficient and suitable to the one line stepper, which turns the company (once was under the law of reconstruction initiated by the banks) to most profitable semiconductor company in the world. As a result of this effort, he was awarded the 'Industrial Service Merit' by President of Korea, Kim DaeJoong in 2002. After leaving the company, he continued to serve as a consultant to the company in the area of reliability enhancement of the DRAM and Flash memory during 2002-2005.

Major Research Achievements

– Advanced Carrier transport modeling

Hybrid method to mix the 'Monte Carlo method" and "drift diffusion model" in the silicon device. The Monte Carlo method is applied to the region where non static transport is important and the drift diffusion model is applied to the regions where the static transport approximation model is valid. The method has been subsequently used by the Stanford group under the name of "Windowed Monte Carlo method".

- ### – TEHED (Tail Electron Hydrodynamic model):
- Developed a hybrid method where the transport of hot carriers having energy higher than a certain energy level of interest (e.g., 1.1eV for impact ionization and 3eV for hot carrier injection toward SiO₂) with the Prof Dutton's group in 1994. The work resulted in the series of papers in IEEE.

– Device and circuit technology

Designed a series of circuits with bulk of the MOSFET devices are controlled by gates. Especially the techniques are applied to the charge pumping circuits to remove the voltage loss due to the back bias effects during the charge transfer to the subsequent stage. The techniques are published in IEEE, J. of Solid State Circuits and filed to Korea patent # 10-0296861-0000 and some part in US #07292089. The technique is now used as the standard charge pumping circuits for most advanced NAND Flash memory more than 70% in the world.

Contributions to Professional Society

- IEEE IEDM; served as the subcommittee member of "CMOS technology" from 2001-2003.
- KITE president of Semiconductor Sector
- Director of Korean national semiconductor project(system 2010 project) from 1999-2001.

Publications - International Journal

1. Y.J.Park, T.W.Tang and D.H. Navon, "Monte Carlo surface scattering simulation in MOSFET structure," IEEE Trans. Electron Dev., Vol.ED-30, No.9, pp.1110-1116, September 1983.

2. Y.J.Park, D.H. Navon, T.W.Tang, "Monte Carlo simulation of bipolar transistors," IEEE Trans. Electron Dev., Vol. ED-31, No.12, pp.1724-1730, December 1984.
3. S.P. Gaur, R.K. Cook, Y.S .Huang, Y.J. Park, and P. Habitz, "Two-dimensional physics simulation of bipolar transistors," IBM Journal of Research and Development, May 1985.
4. Y.J.Park,R.K. Cook, and S.P. Gaur, "The effects of carrier-dependent band gap narrowing on the bipolar device characteristics," IEEE Trans. Electron Dev., Vol.ED-32, No.5, pp.874-876, May, 1985.
5. S.S. Lee, S.D. Lee, S.J. Hong, H.S. Kim, and Y.J. Park, "High-speed EPROM process technology development," Solid State Technology, Vol 30, No.10, pp.149-152, 1987.
6. M.H. Park, D.G. Khang, J.S. Goo and Y.J. Park, "Charge to breakdown mechanism of thin ONO films," IEEE Trans. Electron Dev., November 1990.
7. J.H. Lee, Y.J. Park and J.D. Lee, "Under field oxide dopant enhancement (UFDE) for CMOS and BiCMOS technology," Japanese Journal of Appl. Phys., Vol.22, No.12, 1990.
8. H. Kim, H.S. Min, T.W. Tang and Y.J Park, "An extended proof of the Ramo-Shockley theorem," Solid-State Electronics, Vol.34, No.11, November 1991.
9. G.Y. Jin, Y.J. Park and H.S. Min, "Mixed particle Monte Carlo method for deep submicron semiconductor device simulator," IEEE Trans. CAD/ICAS, Vol.10, No.12, Dec., 1991.
10. J. H. Song, Y. J. Park, H. S. Min, "Detection of the trapped electron distribution of PMOSFETs after hot carrier stress," IEEE Trans. on Electron Devices, Vol. 40, No. 5, pp.958-965, May 1993.
11. K. G. Mo, H. S. Min, Y. J. Park, "Equivalent noise source for Boltzmann transport equation with relaxation time approximation in nondegenerate semiconductors," J. of Applied Physics, Vol. 72, No. 11, November 1993.
12. K. Lee, H. S. Min and Y. J. Park, "Estimation of noise power spectral densities from the Monte-Carlo simulated terminal currents in semiconductor devices," Solid-State Electronics, Vol. 36, No. 11, pp.1263-1270, November 1993.
13. Woo-Hyeong Lee, Young-June Park, and Jong Duk Lee, "A new 0.25 μm recessed channel MOSFET with selectively halo-doped channel and deep graded source/drain," IEEE Electron Device Lett., Vol. 14, December 1993.
14. Woo-Hyeong Lee, Young-June Park, and Jong Duk Lee, "A new recessed channel metal-oxide-semiconductor field-effect transistor with selectively halo-doped channel

and deep graded source/drain," Jpn. J. Appl. Phys. Vol. 33, Part 1, No. 1B, pp.529-531, January 1994.

15. Jong Ho Lee, Young-June Park, and Jong Duk Lee, "Effect of high injection barrier (HIB) on bipolar transistor characteristics," IEEE Trans. on Electron Devices, Vol. 41, no. 1, January 1994.
16. A. Desouki, Y. J. Park and H. S. Min, "Optimization of the bipolar transistor base profile for high-speed BiCMOS circuit," IEEE Trans. CAD/ICAS, Vol. 13, No. 4, pp.471-481, April 1994.
17. J. B. Lee, H. S. Min and Y. J. Park, "Steady-state Nyquist theorem for multi-terminal nondegenerator semiconductor device," J. of Applied Physics, Vol. 75, No. 12, pp.8182-8194, June 1994.
18. W. S. Choi, J. G. Ahn, Y. J. Park and H. S. Min, "A time dependent hydrodynamic device simulator SNU-2D with new discretization scheme and algorithm," IEEE Trans. CAD/ICAS, Vol. 13, No. 7, pp.899-908, July 1994.
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23. Jin-Hyeok Choi, Young-June Park and Hong Shick Min, "Electron mobility behavior in extremely thin SOI MOSFET's," IEEE Electron Device Letters, Vol. 16, No. 11, p.527, November 1995.
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56. Jeong-Hyong Yi, Young June Park, and Hong Shick Min, " Analytical model for and scale-down effect of a floating body voltage in SOI MOSFETs," J. of the Korean Physical Society, Vol. 40, no. 4, pp. 668~671, April 2002.
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influence," IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 49, NO. 4, pp. 605-612, April 2002.

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- International Conference

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